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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/775,908 | 02/10/2004 | Leonard Forbes | 400.272US01 | 1212 |

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| EXAMINER | |
|---|---|
| HO, TU TU V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/775,908 | FORBES, LEONARD | |
| | Examiner | Art Unit | |
| | Tu-Tu Ho | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/02/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Oath/Declaration*

1. The oath/declaration filed on 02/10/2004 is acceptable.

### *Election/ Restriction*

2. Applicant's election without traverse of Invention I, **claims 1-15**, and cancellation of claims 16-34, in the reply filed on 01/24/2005 is acknowledged.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**3.** **Claims 1-2, 5-6, and 9** are rejected under 35 U.S.C. 102(e) as being anticipated by Halliyal et al. U.S. Patent 6,674,138 (the '138 patent).

The '138 patent discloses in Figure 1 and respective portions of the specification an NROM memory transistor as claimed. In particular, the reference discloses a composite gate insulator comprising oxide/high-k dielectric/oxide (28/30/32, column 5, lines 1-15).

Specifically, referring to **claim 1**, the reference discloses an NROM memory transistor comprising:

a substrate (16) having a plurality of source/drain regions (12/14), the source/drain regions (inherently) having a different conductivity type than the remainder of the substrate (for the device to function);

a nanolaminate gate dielectric (28/30/32, which is collectively referred to as 26, having a thickness in the nanometers (column 11, line 64 to column 14), which dimension qualifies the gate dielectric as a nano-laminate gate dielectric or nanolaminate gate dielectric) formed on top of the substrate substantially between the plurality of source/drain regions, the gate dielectric having a dielectric constant greater than silicon dioxide (Table 1 in light of the interpretations in columns 5 and 6); and

a control gate (24) formed on top of the gate dielectric.

Referring to **claim 6** and using the same reference characters, interpretations, and citations as detailed above where applicable, the reference discloses an NROM memory transistor comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;

a composite gate insulator layer formed on top of the substrate and substantially between the plurality of source/drain regions, the gate insulator comprises a trapping layer (high-k dielectric layer 30) having a higher dielectric constant than silicon dioxide (Table 1 in light of the interpretations in columns 5 and 6); and

a control gate formed on top of the gate insulator layer.

Referring to **claim 2**, as noted, the reference discloses that the gate dielectric is a composite oxide - high-k - dielectric - oxide (oxide/high-k dielectric/oxide) nanolaminate gate insulator wherein the high-k dielectric is a charge trapping layer.

Referring to **claim 5**, the reference's disclosed materials meet the Markush group of the claim (Table 1 in light of the interpretations in columns 5 and 6 for the materials and column 13, lines 10-20, for the limitation "ALD")

Referring to **claim 9**, the reference further discloses that the control gate is a polysilicon material (column 4, lines 50-60).

**4.** **Claims 1-2, 6-7, and 9** are rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. U.S. Patent 6,461,949 (the '949 patent).

The '949 patent discloses in the figures, particularly Figure 6, and respective portions of the specification an NROM memory transistor as claimed. In particular, the reference discloses a composite gate insulator comprising oxide/high-k oxide nitride dielectric/high-k tantalum pentaoxide oxide (column 3, lines 1-26).

Specifically, referring to **claim 1**, the reference discloses an NROM memory transistor comprising:

a substrate (52) having a plurality of source/drain regions (64), the source/drain regions (inherently) having a different conductivity type than the remainder of the substrate (see also Description of The Prior Art section);

a nanolaminate gate dielectric (54/56/58, which is collectively referred to as 60, having a thickness of about 15-25 nanometer (or 150-250 angstroms, column 2, lines 55-60), which

dimension qualifies the gate dielectric as a nano-laminate gate dielectric or nanolaminate gate dielectric) formed on top of the substrate substantially between the plurality of source/drain regions, the gate dielectric having a dielectric constant greater than silicon dioxide (column 3, lines 20-25); and

a control gate (68) formed on top of the gate dielectric.

Referring to **claim 6** and using the same reference characters, interpretations, and citations as detailed above where applicable, the reference discloses an NROM memory transistor comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;

a composite gate insulator layer formed on top of the substrate and substantially between the plurality of source/drain regions, the gate insulator comprises a trapping layer (Silicon Nitride (SiN) 56) having a higher dielectric constant than silicon dioxide (column 3, lines 20-28); and

a control gate formed on top of the gate insulator layer.

Referring to **claim 2**, the reference further discloses that the gate dielectric is a composite oxide - high-k - dielectric - oxide nanolaminate gate insulator wherein the high-k dielectric is a charge trapping layer (column 3, lines 15-27).

Referring to **claim 7**, the reference further discloses that the composite gate insulator comprises an oxide - nitride - high-k dielectric structure (column 3, lines 15-27).

Referring to **claim 9**, the reference further discloses that the control gate is a polysilicon material (column 3, lines 46-49).

5. **Claims 1-2, 6-7, and 9** are rejected under 35 U.S.C. 102(e) as being anticipated by Chang U.S. Patent 6,797,567 (the '567 patent).

The '567 patent discloses in the figures, particularly Figure 1E, and respective portions of the specification an NROM memory transistor as claimed. In particular, the reference discloses a composite gate insulator comprising high-k HfOxNy/high-k silicon nitride dielectric/oxide (102/104/106 that to become 102a/104a/106a, column 3, line 60, to column 4, line 35).

Specifically, referring to **claim 1**, the reference discloses an NROM memory transistor comprising:

a substrate (100) having a plurality of source/drain regions (114), the source/drain regions (inherently) having a different conductivity type than the remainder of the substrate (for the device to function);

a nanolaminate gate dielectric (102a/104a/106a, which is collectively referred to as 108, having a thickness in the nanometers, as is known in the art and as is disclosed or proved by the other references cited by the examiner), which dimension qualifies the gate dielectric as a nano-laminate gate dielectric or nanolaminate gate dielectric) formed on top of the substrate substantially between the plurality of source/drain regions, the gate dielectric having a dielectric constant greater than silicon dioxide (column 3, lines 60-67); and

a control gate ("word line" 118) formed on top of the gate dielectric.

Referring to **claim 6** and using the same reference characters, interpretations, and citations as detailed above where applicable, the reference discloses an NROM memory transistor comprising:

a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate;

a composite gate insulator layer formed on top of the substrate and substantially between the plurality of source/drain regions, the gate insulator comprises a trapping layer (Silicon Nitride 104) having a higher dielectric constant than silicon dioxide (see Table 1 of the '138 patent for a disclosure that silicon nitride has a higher dielectric constant than silicon dioxide); and

a control gate formed on top of the gate insulator layer.

Referring to **claim 2**, as noted, the reference discloses that the gate dielectric is a composite oxide - high-k - dielectric - oxide (high-k HfOxNy oxide/high-k silicon nitride dielectric/oxide) nanolaminate gate insulator wherein the high-k dielectric is a charge trapping layer (column 3, lines 15-27).

Referring to **claim 7**, as noted, the reference discloses that the composite gate insulator comprises an oxide - nitride - high-k dielectric structure (high-k HfOxNy dielectric/high-k silicon nitride dielectric/oxide, as direction of the layers of the composite layer has not been established in the claim).

Referring to **claim 9**, the reference further discloses that the control gate is a polysilicon material (column 4, lines 50-60).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**6.** **Claims 15, 8, and 10** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '949 patent.

Referring to **claim 15**, the '949 patent discloses a plurality of NROM memory transistors as claimed and as detailed above but fails to teach that the plurality of NROM memory transistors could be used in an electronic system having a process and a memory array of the plurality of NROM memory transistors. However, since the reference also fails to exclude such usage, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory array of the plurality of NROM memory transistors in an electronic system having a process as it was known at the time the invention was made that a memory array needed to be coupled to a processor of sorts to function.

Referring to **claim 8**, although the reference fails to disclose a specific doping for the source/drain regions as claimed, n+ type doped silicon is a popular doping and that one in that art would use. See, for example, column 1, lines 28-35.

Referring to **claim 10**, the reference further discloses that the substrate 52 is comprised of p-type silicon (column 2, lines 52-54). In other words, the difference between the reference and the claim appears to be that of the p-dopant: the claim recites p+, the reference just p or p-. However, since both the reference and the claim fail to explicitly disclose a specific concentration (doping concentration or impurity concentration, as is known in the art), the choosing of terminology and even doping concentration is all within the skill of one in the art therefore such a choosing would have been obvious.

7. **Claim 11** is rejected under 35 U.S.C. §103(a) as being unpatentable over the '949 patent in view of knowledge in the art and further in view of knowledge in the art or further in view of Min U.S. Patent 6,669,990 (the '990 patent).

The reference discloses an NROM memory transistor as claimed and as detailed above including the high-k composite gate insulator. The difference between the reference's structure and that of the claim is the top oxide layer of the composite gate insulator. The claim recites a high-k atomic-layer-deposition (ALD) aluminum oxide ($Al_2O_3$) or ALD zirconium oxide ($ZrO_2$), the reference discloses the high-k tantalum pentaoxide ($TaO_5$), or simply "tantalum oxide" for short.

However, with reference to the materials, the different materials are just high-k materials one of ordinary skill in the art would use for gate insulator and therefore would have been obvious. See, for example, Table 1 of U.S. Patent 6,674,138 to Halliyal et al., which details the equivalency of the different materials.

With respect to the limitation "ALD" in the materials, the limitation appears to refer to the process (atomic layer deposition) by which the material is formed. Nevertheless, (1) the process limitation in a product, which is popularly referred to as a "product-by-process limitation" has been found immaterial to the patentability of the process. (2) In addition, ALD, at the time the invention was made, already was known for its superiority in forming high-k materials, specifically high-k gate insulator ("high-k gate oxide"), such as uniformity of composition and thickness, over other processes. See, for example, Min U.S. Patent 6,669,990,

column 1, lines 22-29). It is therefore clear that either (1) or (2) listed above would render the claim unpatentable.

*Claim Rejections - 35 USC §102 or 103*

8. **Claims 3 and 4** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over the '138 patent.

The reference discloses a device and materials as claimed and as detailed above for claims 1 and 5, and since the reference's structure and materials are similar or substantially similar to that to the claims, there is no reason to believe that the structure does not possesses the properties as claimed.

9. **Claims 1-4, 6-10, 12-13, and 15** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kinoshita et al. U.S. Patent 6,780,708 (the '708 patent).

The '708 patent, in disclosing a method of forming core and peripheral gates, teaches an NROM memory transistor comprising a layer of nanolaminate or composite gate insulator or dielectric consisting of tunneling layer/charge-trapping layer/insulating layer 28/30/32, any one of which could be a high-k dielectric layer (Fig. 6 and column 7, lines 7-14, column 8, lines 25-40), where, as should be apparent by now and as disclosed also in column 9, lines 20-29) the high-k dielectric has a dielectric constant greater than that of silicon dioxide. The reference further teaches that the incomplete device as depicted in Fig. 6 may be completed by conventional techniques to form required features such as dopants, source/drain regions and the

like (column 14, lines 41+). In other words, the reference disclose an NROM memory transistor as claimed or substantially as claimed in these claims. See the preceding paragraphs for other critical, or optional (such as a processor to work with the memory device), but not disclosed, elements for the device to function and the inherent band edge or energy barrier characteristics when the materials of the respective layers are similar to the claimed.

**10.** **Claims 1-15** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Hoefler et al. U.S. Patent 6,713,812 (the '812 patent).

The '812 patent discloses in the figures, particularly Fig. 4, and respective portions of the specification an NROM memory transistor that appears to have more limitations than the claims. For example, the reference discloses a composite substrate 12/16/20 having alternating and opposite conductivity types and a pair of source/drain regions that has an n-type conductivity (paragraph bridging columns 5 and 6); therefore it can not be said that the reference discloses "a substrate having a plurality of source/drain regions, the source/drain regions having a different conductivity than the remainder of the substrate" as claimed in the independent claims. However, if one considers "substrate" broadly, for example, just the p-well 20 (column 2,lines 45-46), then the reference anticipates the limitations of the claims. In the alternative, since the extra layers of the substrate of the reference, or the lack of them, do not result in unexpected outcomes of the device therefore the removing of the extra layers or the adding of them would not constitute patentability.

The reference further discloses that the NROM memory transistor depicted in the figures comprises a layer of nanolaminate or composite gate insulator or dielectric consisting of

tunneling layer/charge-trapping layer/inter-gate insulating layer 40/38/36, any one of which could be a high-k dielectric layer - (i.e., oxynitride or metal oxide, Fig. 4 and column 4, lines 1-14), where, as should be apparent by now and as disclosed in Table 1, in light of the interpretations in columns 5 and 6, of the '138 patent, that the high-k dielectric has a dielectric constant greater than that of silicon dioxide - and any one of which could be formed by ALD (column 3, lines 34-55). In the alternative, it would have been obvious to one of ordinary skills in the art at the time the invention was made to change the respective layers, i.e., tunneling layer, charge-trapping layer, and inter-gate insulating layer of the '812 patent, so that each of the layers are high-k dielectric layer, in view of the advantages given by the '567 patent, the '138 patent, and the '949 patent, respectively (see the preceding paragraphs for more details about these references). Specifically, the '567 patent teaches that by using a high-k dielectric layer for a tunneling layer, one would obtain, among other advantages, the loss of electrons into the substrate ('the 567 patent, column 5, lines 45-50); the '138 patent teaches that by using a high-k dielectric layer for a charge-trapping layer, one would obtain, among other advantages, reduced dimensions without degrading leakage current (column 4, lines 4-10); and the '949 patent teaches that by using a high-k dielectric layer for an inter-gate insulating layer ("top oxide layer"), one would obtain, among other advantages, a solution to the conventional structure problems of high temperature processing and high cost (column 2, lines 1-21). See the preceding paragraphs for other critical, or optional (such as a processor to work with the memory device), but not disclosed, elements for the device to function and the inherent band edge or energy barrier characteristics when the materials of the respective layers are similar to the claimed.

*Conclusion*

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
February 17, 2005